

A second embodiment of the present invention is shown in Fig.7 in which the same numerals as those of the first embodiment designate the same elements. A semiconductor device 11 includes a packaging substrate 12A and a chip 13 mounted thereon. The packaging substrate 12A includes a central core layer 211 sandwiched between a pair of buildup layers 212, 213, and a plenty of interconnect pads 21 made of a conductive film are formed on the top buildup layer 212. The interconnect pads 21 are connected to the interconnect lines in each of the multi-layers of the top buildup layer 212, further connected to the bottom buildup layer 213 through intermediary of via plugs, and still further connected to ball electrodes 24 formed on the bottom surface of the bottom buildup layer 213 or the bottom surface of the packaging substrate 12A.

Each of the buildup layers is multi-layered, and the top buildup layer 212 includes five interconnect layers in which a first layer includes the interconnect pads 21 and a ground (GND) layer, a third layer includes a GND layer 3G and a voltage (VDD) layer 3V, and a fifth layer includes a GND layer 5G and a VDD layer 5V connected to the via plugs of the above core layer.

IN THE CLAIMS:

Please amend claim 3 as follows, without prejudice:

3. (Once amended) The semiconductor device as defined in claim 1, wherein the mounting member is a semiconductor package for mounting, a semiconductor chip on a packaging substrate, the electrode terminals are ball electrodes disposed on a bottom surface  
*(1/2 b/t the ball electrode & the substrate)*  
*are on the bottom of the substrate, not*  
*locking substrate, substrate.*
- on the ball electrode of the substrate*  
*be on the bottom of the substrate is also*  
*walls, the substrate is also*  
*the package?*